

App. Serial No 10/529,731  
GB020239US1

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**LISTING OF THE CLAIMS**

Please amend claims 1-10 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) An insulated gate power transistor semiconductor device (3) comprising a semiconductor body (10) having an active area with a plurality of electrically parallel transistor cells (TC3), wherein each transistor cell (TC3) has a source region (16) and a drain region (12) of a first conductivity type which are separated by a channel-accommodating body region (23) adjacent an insulated gate structure (G31,32), said gate structure (G31,32) comprising first (G31) and second (G32) gates isolated from each other so as to be independently operable, the first gate (G31) being an insulated trench-gate (21,22) adjacent the body region (23) enabling a first, vertical, channel portion (23b) to be formed in said body portion (23) when gate potential is applied to the first gate (G31), the second gate (G32) having at least an insulated planar gate portion (13,14) on a top major surface (10a) of the semiconductor body (10) adjacent the body region (23) enabling a second, at least partly lateral, channel portion (23e) to be formed in said body portion (23) when gate potential is applied to the second gate (G32), such that simultaneous operation of the first (G31) and second (G32) gates combines the first and second channel portions (23b, 23e) to form a conduction channel between the source (16) and drain (12) regions.

2. (Currently amended) A semiconductor device (3) as claimed in claim 1, wherein a said gate structure (G31,32) is located at the boundary between each two adjacent transistor cells (TC3), wherein at said boundary, an insulated trench (20,21) having gate material (22) therein forms said first gate (G31) for the two transistor cells, and a planar insulation layer (13) with gate material (14) thereon is located on top of the trench (20) and extends laterally both ways beyond the trench (20), such that said second gate (G32) for the two transistor cells is an insulated substantially completely planar gate, and such that the planar insulation layer (13) also isolates the first (G31) and second (G32) gates from each other for the two transistor cells.

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3. (Currently amended) A semiconductor device (4) as claimed in claim 1, wherein a said gate structure (G41,42) is located at the boundary between the two adjacent transistor cells (TC4), wherein at said boundary, an insulated trench (20,21) having gate material (22a) in a lower portion of the trench (20) provides said first gate (G41) for the two transistor cells, a first insulation layer (13a) is located laterally within and across the trench (20) with gate material (14a) thereon in an upper part of the trench (20), and a second insulation layer (13b) with gate material (14b) thereon extends laterally both ways from the trench (20) on the top major surface (10a) of the semiconductor body (10), such that said second gate (G42) for the two transistor cells has an insulated trench-gate portion and an insulated planar gate portion, and such that the first insulation layer (13a) laterally within and across the trench (20) isolates the first (G41) and second (G42) gates from each other for the two transistor cells.

4. (Currently amended) A semiconductor device as claimed in any one of claims 1 to 3, wherein the transistor cells (TC3, TC4) in the active area have a closed cell geometry in which said peripheral gate structures surround each transistor cell in a two-dimensionally repetitive pattern.

5. (Currently amended) A circuit arrangement (50,60) including a power transistor semiconductor device (3,4) as claimed in ~~any one of claim~~[[s]] 1 to 4, wherein the first gates (G31) and the second gates (G32) of the transistor cells are respectively connected to first (G311) and second (G321) gate electrodes of the device, and wherein said first (G311) and second (G321) gate electrodes are arranged for connection to respective independent applied control potentials (Vcc, VF; 573,673).

6. (Currently amended) A circuit arrangement (50,60) as claimed in claim 5, wherein terminal means (Vcc, VF) for connecting to a supplied a fixed gate potential is connected to the first gate electrode (G311), and wherein a gate driver circuit (573,673) for applying a modulating gate potential is connected to the second gate electrode (G321).

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7. (Currently amended) A circuit arrangement (~~50~~) as claimed in claim 6, wherein the power transistor semiconductor device is a high side power transistor (~~3,4~~) connected in series with a low side power transistor (~~6~~) for supplying a regulated voltage to an output (~~51~~) via a switch node (~~52~~) connection between the high side (~~3~~) and low side (~~6~~) transistors, and wherein said gate driver circuit (~~573~~) is included in a control circuit (~~57~~) for alternately switching the high side (~~3,4~~) and low side (~~6~~) transistors on and off.

8. (Currently amended) A circuit arrangement (~~60~~) as claimed in claim 6, wherein the power transistor semiconductor device is a switch (~~3,4~~) for supplying current to a load (L) when the load (L) is connected to one of a source electrode and a drain electrode of the device.

9. (Currently amended) A circuit arrangement (~~60~~) as claimed in claim 8, wherein the gate driver circuit (~~673~~) is included in a control circuit (~~67~~) which is integrated with the power transistor switch (~~3,4~~) in said semiconductor body (~~10~~).

10. (Currently amended) A circuit arrangement (~~60~~) as claimed in claim 9, wherein the control circuit (~~67~~) includes protection circuit means (~~674~~) for the power transistor switch (~~3,4~~).